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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,263	12/02/2003	Richard Fournel	61170-00025USPX	3373

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EXAMINER	
NGUYEN, TUAN T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,263	FOURNEL ET AL.	
	Examiner	Art Unit	
	Tuan T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-18* is/are allowed.

6)☒ Claim(s) *1-8 and 10-12* is/are rejected.

7)☒ Claim(s) *9 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

1/23/06

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/4/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history printout*.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 3/4/04 was filed after the mailing date of the present application on 12/2/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

3. Claims **6** and **9** are objected to because of the following informalities:

Claim **6**, line 4, "DC voltage supply source" should read as – DC voltage reference –

Claim **9**, line 2, "the said NMOS" should read as – said NMOS --

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims **1-8, 10-12** are rejected under 35 U.S.C. 102(b) as being anticipated by Hirose et al (US 5,892,172).

Hirose et al disclose a nonvolatile SRAM (figures 1-2) comprising first (14) and second (14') inverters interconnected between first (104) and second (104') data nodes, each inverter comprising complimentary MOS transistors (PMOS 10, 10', NMOS 11, 11') connected in series between a DC voltage reference (Vcc) and a ground reference (101), means (NV1, NV2) for programming the MOS transistors adapted for causing, after programming, an irreversible degradation of a gate oxide layer of at least one of the transistors (see column 5, lines 22-67, column 6, lines 1-67) as recited in claims **1-4.**

Regarding claim **5**, Hirose et al show a programming control line as Cg connected to gate of NMOS transistors NV1, NV2 (13, 13')

Regarding claim **6**, the programming voltage reference would be voltage potential at node 104 or node 104'.

Regarding claim **7**, Hirose et al also show a means (NV1 23, and NV2 23' in Fig. 2) for causing the cell to operate as an SRAM memory after programming.

Regarding claim **8**, a control line would be Cg 205 in Hirose et al's Fig. 2.

Regarding claims **10-11**, pair of load resistor would be 10 and 10', a programming circuit would be NV1 and NV2 in Hirose et al's Fig. 1

Regarding claim **12**, first programming transistor would be transistor 13' and second programming transistor would be transistor 13 in Hirose et al's Fig. 1.

Allowable Subject Matter

6. Claims **14-18** are allowed.

7. Claims **9 and 13** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is an examiner's statement of reasons for allowance:

The prior art of record ((Hirose et al US 5,982,712; Hirose et al. US 6,122,191; and Choi US 2003/0179630) fail to disclose an SRAM memory cell of the 6T type including a pair of inverter transistors which are cross-coupled and a pair of load transistors, the memory cell further including a operational configuration circuit that selectively connects and disconnects a gate of a first load transistor to a gate of a first inverter transistor and selectively connects and disconnects a gate of a second load transistor to a gate of a second inverter transistor as recited in claim **14**.

Claims **15-18** are therefore allowed because of their dependency on claim **14**.

9. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fail to disclose an SRAM memory cell of claim **8,** wherein a drain and source electrode of each of the NMOS transistors are respectively linked to the gate of the transistors of one of the inverters as recited in claim **9**.

The prior art of record further fail to disclose the SRAM of claim **12**, wherein the first and second programming transistors are connected in series with each other as recited in claim **13.**

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Nguyen whose telephone number is 571-272-1880. The examiner can normally be reached on Monday - Friday, 8AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T Nguyen
Examiner
Art Unit 2824

January 23, 2006